Operation of Multilevel Inverters under Unbalanced DC Sources Using Neutral Voltage Modulation

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Abstract: This paper explains the operation of multilevel inverters under unbalanced dc sources. To control the multilevel inverters under unbalanced dc sources three different pulse width modulation techniques were used. Under these three modulation techniques the operation of multilevel inverters was observed. The difference between the three modulation techniques by concentrating on the balanced line to line voltages and balanced output currents is explained. The linear modulation range is reduced under unbalanced DC link conditions. To maximize the linear modulation range, neutral voltage modulation technique is used. Total harmonic distortion for a seven level cascaded inverter with unbalanced dc sources by using three different modulation techniques is explained.

Keywords: Multilevel cascaded inverters (MLCIs), neutral voltage modulation (NVM), phase shifted (PS), pulse width modulation (PWM), space vector pulse width modulation (SVPWM), total harmonic distortion (THD)

I. INTRODUCTION

Multilevel means several steps. So, multilevel inverter gives the output voltage in the form of several steps, which is the synthesis of an output voltage in the form of sinusoidal. dv/dt characteristics of multilevel inverters are low. Voltage and current harmonics are low compared to single level. We can achieve high voltages by combing multilevel modules [1]-[4]. By considering above advantages these inverters are employed in different applications [5]-[8]. There are various multilevel inverter topologies [9]. Among these multilevel cascaded [MLCI] structure is very prominent topology. MLCIs structure is simple and has a good capability of fault-tolerant. Due to these advantages multilevel cascaded inverters are used in different applications such as voltage restorer, synchronous compensator, storage device of high level energy etc [10]-[15]. In MLCIs gating signal control for switches is very important. For this different modulation techniques are proposed. They are categorized as selective harmonic elimination (SHEPWM), carrier based and space vector (SVPWM) [16]. For motor drives a carrier based PWM or SVPWM is used, because the dynamic properties are most important in motor drives. In static power converters SHEPWM is used. For easy implementation of SVPWM to MLCIs a series SVPWM method has been proposed in [17].

MLCIs consists equal number of cells in each phase. If any fault occurs in one or two phases, the output voltages will be unbalanced. To rectify this problem a switch diverter is placed across each switch in each phase. To balance the output voltage, the fault occurred cells are diverted and along with faulty cells the remaining phase cells are also diverted. Due to this the output voltages are balanced but the magnitude of the voltages is very low. To eliminate above problem a neutral shift method is produced in which the reference neutral axis is shifted and the phase voltages with different phase shifts [18]. But above incidents are dealing with the phase faults. MLCIs require separate DC sources. If any fault occurs in DC links or if the magnitude of DC sources is different the output of MLCIs will be unbalanced. To deal with this issue some studies have been conducted. In multilevel inverters under faulty conditions there is a reduction in modulation index on switches as in [19] and proposed a compensation algorithm for phase shifted PWM. A new method called duty cycle modification is introduced to balance the output voltage for single phase power fluctuations in [20]. Another technique an offset voltage injection is proposed to balance the output voltage. But introducing integrator may reduce dynamic characteristics In this paper, to maximize linear modulation range and to balance line to line voltages of a multilevel inverter operating with unequal dc voltages, a carrier based PWM strategy is explained. Under unequal dc-link conditions, the maximum phase voltage in each phase is non uniform. Consequently, reduction in linear modulation range and imbalance of output voltage can occurs as references of output voltages are increases. To explain the theory behind the unbalance in output voltages, the voltage space vector for MLCI is evaluated. And also by considering the unbalanced dc sources, linear modulation range is explained. After that a neutral voltage modulation technique is explained. This method is useful to balancing of output voltage as well as to increase the linear modulation index up to maximum extant point. In this technique, the reference of neutral voltage,

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which takes a zero sequence voltage to compress the voltage imbalance, and to extend the modulation range an offset voltage is taken into account. The results obtained by using this neutral voltage modulation technique are compared with the results obtained by applying traditional PWM and space vector PWM. And results are observed what happens if the duty cycles are increased

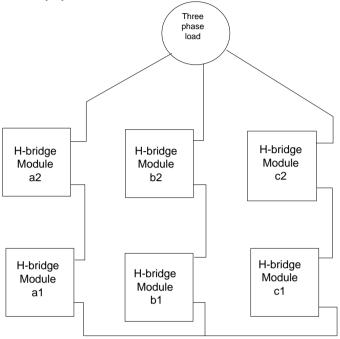


Fig.1. schematic diagram of MLCI

Fig. 1 shows the basic configuration of multilevel cascaded inverter. With this configuration, different power ratings can be easily obtained by connecting the number of H bridges according to required specifications. Here, H bridge model consists of current and voltage sensors circuits, gate driver and main controller. Each H bridge module has separate dc link or battery. Between two switching a unipolar modulation technique is applied. In H Bridge the switching frequency is twice to that of carrier signal. To implement multilevel operation and interleaving, the PS shifted modulation is used [22]. The switching frequency in a phase is,

$$f_{switc h} = 2N * f_c$$

Where, N=number of H bridge models and f_c = frequency of carrier signal

II. Space Vector Analysis of Voltage

Let, single H bridge module has dc link voltage as V_{dc} and output voltage as v_{pn} . Output has three stages, i.e. V_{dc} , 0 and $-V_{dc}$ as shown in Fig.2. The switching function can be represented as

$$\begin{aligned} v_{pn} &= S_p V_{dc} \\ S_p & \epsilon \{-1,0,1\}_{p=a,b \text{ or } c} \end{aligned}$$

Where S_p is function of switching and a, b and c are phases.

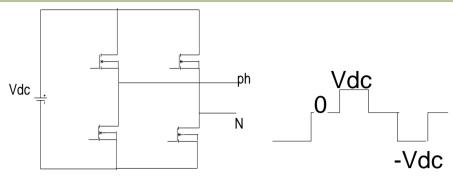


Fig.2. single H bridge circuit and output

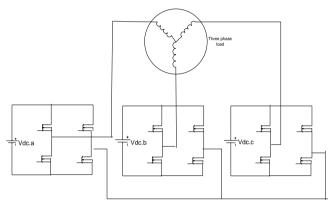


Fig.3. one-by-three configuration

Fig.3 shows a MLCI of one-by-three configuration. For voltage analysis, main concept is derived and is expanded to more levels. There are two neutral points in the circuit named as I and n. The voltage between the output point and neutral point is called as pole voltage. The pole voltages are named v_{cn} as v_{an} , v_{bn} and v_{cn} . Voltage between output point and load neutral point is called as phase voltages v_{al} , v_{bl} and v_{cl} . The difference between two neutral point voltages can be write as

$$v_{ln} = -v_{al} + v_{an} = -v_{bl} + v_{bn} = -v_{cl} + v_{cn}$$

If there is no neutral point the sum of phase voltages is zero then the voltage between two neutral points is written as

$$v_{ln} = \frac{1}{3}(v_{an} + v_{bn} + v_{cn})$$

By using (4), (3) can be re written as

$$v_{al} = \frac{2}{3} S_a V_{dc_a} - \frac{1}{3} S_b V_{dc_b} - \frac{1}{3} S_c V_{dc_c}$$

$$v_{bl} = -\frac{1}{3} S_a V_{dc_a} + \frac{2}{3} S_b V_{dc_b} - \frac{1}{3} S_c V_{dc_c}$$

$$v_{cl} = -\frac{1}{3} S_a V_{dc_a} - \frac{1}{3} S_b V_{dc_b} + \frac{2}{3} S_c V_{dc_c}$$

Where S_a , S_b and S_c are switching functions of the phases a, b and c. based on these switching functions different levels of voltage are obtained. The maximum amplitude of the phase voltage $V_{ph.max}$ is given by $V_{ph.max} = \frac{V_{dc.mid} + V_{dc.min}}{\sqrt{3}}$ different levels of voltage are obtained.

$$V_{ph.max} = \frac{V_{dc.mid} + V_{dc.min}}{\sqrt{3}}$$

If all the three sources in the Fig.3 are balanced or equal to V_{dc} , then the maximum amplitude of phase voltage

is given as
$$V_{ph.max} = \frac{2}{\sqrt{3}} V_{dc}$$

We calculate the duty cycles for all the three types of modulation techniques and compare them with the phase shifted carrier waves as shown in Fig.4.

III. **Modulation Techniques**

Traditional Pulse Width Modulation

In this traditional pulse width modulation technique, we assume that the voltage difference between the two neutral points is zero. So, the reference neutral voltage is taken as zero and the reference phase voltages directly given to duty cycle production algorithm.

$$v_{ln}^* = 0$$

Traditional SVPWM

In this space vector pulse width modulation technique, the voltage difference between the two neutral points is considered. But it is assume that this neutral voltage is constant. The neutral point voltage is calculated

$$\begin{aligned} v_{ln}^* &= \frac{v_{max}^* + v_{min}^*}{2} \\ v_{max}^* &= max(v_{al}^*, v_{bl}^*, v_{cl}^*) \\ v_{min}^* &= min(v_{al}^*, v_{bl}^*, v_{cl}^*) \end{aligned}$$

By using above equations the reference pole voltages are calculated as $v_{an}^* = v_{al}^* - v_{ln}^*, \quad v_{bn}^* = v_{bl}^* - v_{ln}^*, \quad v_{cn}^* = v_{cl}^* - v_{ln}^*$ These reference voltages are used for the duty calculation

$$v_{an}^* = v_{al}^* - v_{ln}^*$$
, $v_{bn}^* = v_{bl}^* - v_{ln}^*$, $v_{cn}^* = v_{cl}^* - v_{ln}^*$

Neutral Voltage Modulation Technique

In this type of modulation technique, the neutral voltage between two points is modulated to balance the output voltage under unbalanced dc link conditions. For this, the weight constants are introduced. The weight constant is calculated as

$$C_w = \frac{V_{dc.mid} + V_{dc.min}}{2}$$

$$C_{w_b} = \frac{c_w}{v_{dc_b}}$$
 $C_{w_a} = \frac{c_w}{v_{dc_a}}$ $C_{w_c} = \frac{c_w}{v_{dc_c}}$

By using this, the weight factors for each phase are calculated as $C_{w_b} = \frac{C_w}{V_{dc_b}} \qquad C_{w_a} = \frac{C_w}{V_{dc_a}} \qquad C_{w_c} = \frac{C_w}{V_{dc_c}}$ These weighted factors are multiplied with the reference phase voltages to produce new reference voltages as shown below

$$v'_{al} = C_{w_a} v^*_{al}$$
 $v'_{bl} = C_{w_b} v^*_{bl}$ $v'_{cl} = C_{w_c} v^*_{cl}$
By using these reference voltages, the reference neutral voltage is calculated as $v'_{cl} = min(v'_{cl}, v'_{cl}, v'_{cl})$ $v'_{cl} = max(v'_{cl}, v'_{cl}, v'_{cl})$

$$v_{min}' = min(v_{al}', v_{bl}', v_{cl}')$$
 $v_{max}' = max(v_{al}', v_{bl}', v_{cl}')$

$$v_{ln}' = \frac{v_{max}' + v_{min}'}{2}$$

$$v_{an}^* = v_{al}^* - v_{ln}'$$
 $v_{bn}^* = v_{bl}^* - v_{ln}'$, $v_{cn}^* = v_{cl}^* - v_{ln}'$

The above reference pole voltages are given to the duty calculation.

Duty Calculation

The final reference voltages in every type of modulation technique are used to calculate duty cycle as shown in Fig.4.

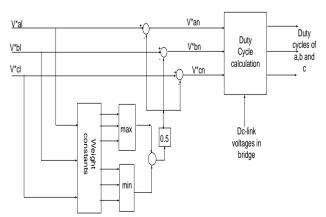


Fig.4. Control algorithm of NVM method

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$$d_{a1}^* = d_{a2}^* \dots \dots = d_{aN}^* = rac{v_{an}^*}{V_{dc.a}}$$
 $d_{b1}^* = d_{b2}^* \dots \dots = d_{bN}^* = rac{v_{bn}^*}{V_{dc.b}}$
 $d_{c1}^* = d_{c2}^* \dots = d_{cN}^* = rac{v_{cn}^*}{V_{dc.c}}$

These calculated duty cycles are compared with the phase shifted carrier to produce pulses to the inverter.

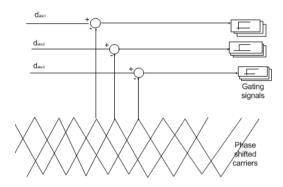


Fig.5. pulse production technique

IV. **Simulation Results**

A simple one-by-three configuration MLCI model is created in MATLAB simulink as shown in Fig.3. The load with R=0.10hm and L=1mH is connected to the MLCI. The values of three dc links are given as $V_{dc.a}=15V$, $V_{dc.b}=22.5V$ and $V_{dc.c}=30V$. The switching frequency of carrier wave is 5KHZ. Therefore the maximum amplitude of phase voltage is given as $V_{ph.max}=\frac{V_{dc.min}+V_{dc.min}}{\sqrt{3}}$

$$V_{ph.max} = \frac{V_{dc.mid} + V_{dc.min}}{\sqrt{3}}$$

$$V_{ph.max} = \frac{22.5 + 15}{\sqrt{3}} = 21.65 \text{V}$$

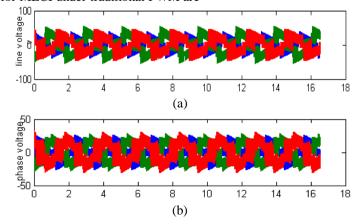
The reference voltages are given as

$$\begin{split} v_{al}^* &= 21.65 sin(100\pi t) \\ v_{bl}^* &= 21.65 sin\left(100\pi t - \frac{2\pi}{3}\right) \\ v_{cl}^* &= 21.65 sin\left(100\pi t + \frac{2\pi}{3}\right) \end{split}$$

By using above conditions the MLCI is operated under three different conditions. The results are explained below.

Traditional PWM

The simulation results for MLCI under traditional PWM are



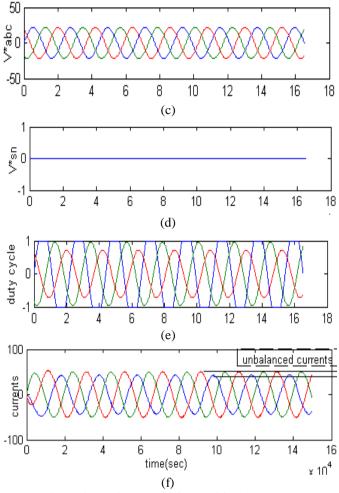


Fig.6. simulation results for traditional PWM\\

From Fig.6 (d) we observe that the neutral voltage is zero. Due to this the reference voltages are pure sinusoidal as shown in Fig. 6 \odot . The line and phase voltages are shown in Fig. 6(a) and (b). The output currents in this method are considerably unbalanced as shown in Fig. 6(f). The total harmonic distortion in the phase voltages is shown in the fig.7 below.

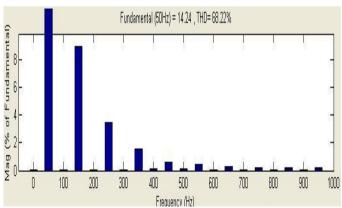


Fig.7. THD of phase voltage in traditional PWM

From Fig.7 the THD of phase voltage is 68.72% in traditional PWM, which is very high.

Traditional SVPWM

The simulation results of traditional SVPWM is shown in the Fig.8.

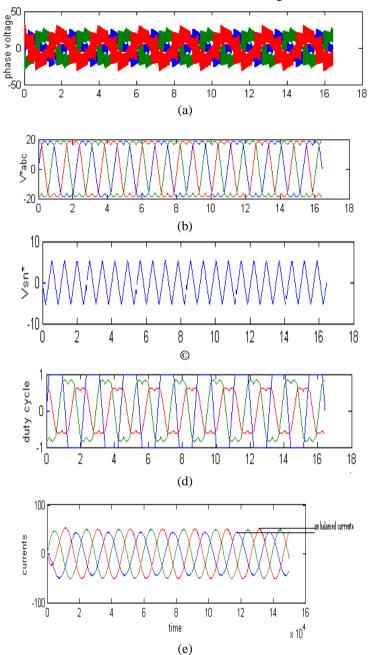


Fig.8. simulation results of traditional SVPWM

The phase voltage of MLCI by SVPWM is shown in Fig. 8(a).

The neutral voltage in this modulation technique is variable between two values as shown in fig.6 ©. Due to this neutral voltage the reference voltages are as shown in Fig. 8 (b). The line currents of inverters are shown in fig.8(e). it is observed that the currents are unbalanced.

The total harmonic distortion of the inverter is shown in Fig.9.

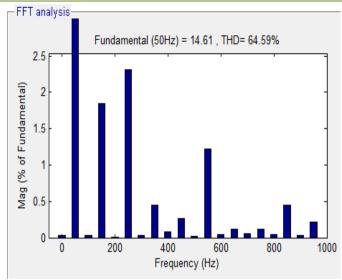
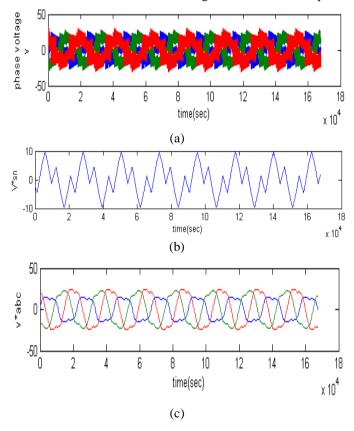


Fig.9 THD of MLCI by SVPWM

The THD of MLCI under traditional SVPWM is 64.59% which is better than traditional PWM but it is also very high.

Neutral voltage modulation technique

The simulation results for MLCI under neutral voltage modulation technique are shown in Fig 10



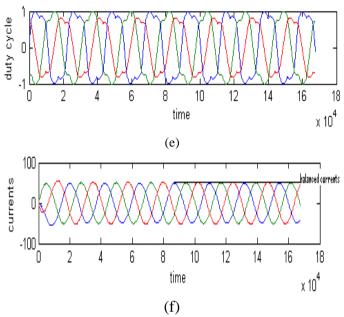


Fig.10. simulation results of neutral voltage modulation technique

Fig.10 (a) shows the phase voltage of multilevel inverter under voltage modulation technique. The voltage difference between two neutral points is varied among different values as shown in Fig, 10 (b). the reference voltages are shown in fig.10 (c). the line currents in this neutral voltage modulation technique is balanced as shown in fig 10(f).

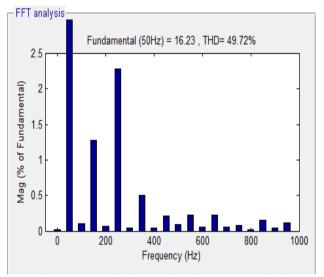


Fig.11. THD of phase voltage in NVM method

The THD of phase voltage in neutral voltage modulation technique is shown in Fig.11. it is 49.72% which is almost 15% lesser than the traditional SVPWM.

V. Conclusion

The multilevel cascaded inverter under unbalanced dc sources exhibits unbalance in the output voltage and current. Three modulation techniques named traditional PWM, traditional SVPWM and neutral voltage modulation technique are applied to eliminate these problems but among these three techniques neutral voltage modulation technique gives better balanced output compared to others. The THD in the output voltage in neutral voltage modulation technique is very less compared to before two

VI. References

- [1]. J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [2]. H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters—State of the art, challenges, and requirements in industrial applications," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2581–2596, Aug. 2010.
- [3]. J.-S. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters," IEEE Trans. Ind. Appl., vol. 32, no. 3, pp. 509–517, May/Jun. 1996.
- [4]. M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2197–2206, Jul. 2010
- [5]. G. Bergna, E. Berne, P. Egrot, P. Lefranc, A. Arzande, J.-C. Vannier, and M. Molinas, "An energy-based controller for HVDC modular multilevel converter in decoupled double synchronous reference frame for voltage oscillation reduction," IEEE Trans. Ind. Electron., vol. 60, no. 6, pp. 2360–2371, Jun. 2013.
- [6]. G. Buticchi, E. Lorenzani, and G. Franceschini, "A five-level single-phase grid-connected converter for renewable distributed systems," IEEE Trans. Ind. Electron., vol. 60, no. 3, pp. 906–918, Mar. 2013
- [7]. Z. Shu, N. Ding, J. Chen, H. Zhu, and X. He, "Multilevel SVPWM with DC-link capacitor voltage balancing control for diode-clamped multilevel converter based STATCOM," IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 1884–1896, May 2013.
- [8]. J. Chavarria, D. Biel, F. Guinjoan, C. Meza, and J. J. Negroni, "Energybalance control of PV cascaded multilevel grid-connected inverters under level-shifted and phase-shifted PWMs," IEEE Trans. Ind. Electron., vol. 60, no. 1, pp. 98–111, Jan. 2013.
- [9]. J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. León, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," Proc. IEEE, vol. 97, no. 11, pp. 1786–1817, Nov. 2009
- [10]. S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, and B. Wu, "Recent advances and industrial applications of multilevel converters," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
- [11]. A. M. Massoud, S. Ahmed, P. N. Enjeti, and B. W. Williams, "Evaluation of a multilevel cascaded-type dynamic voltage restorer employing discontinuous space vector modulation," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2398–2410, Jul. 2010.
- [12]. M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel PWM inverter," IEEE Trans. Power Electron., vol. 25, no. 7, pp. 1786–1799, Jul. 2010.
- [13]. J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930–2945, Dec. 2007.
- [14]. L. Maharjan, S. Inoue, and H. Akagi, "A transformerless energy storage system based on a cascade multilevel PWM converter with star configuration," IEEE Trans. Ind. Appl., vol. 44, no. 5, pp. 1621–1630, Sep./Oct. 2008.
- [15]. W. Song and A. Q. Huang, "Fault-tolerant design and control strategy for cascaded H-bridge multilevel converter-based STATCOM," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2700–2708, Aug. 2010.
- [16]. M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2197–2206, Jul. 2010.
- [17]. R. Rabinovici, D. Baimel, J. Tomasik, and A. Zuckerberger, "Series space vector modulation for multi-level cascaded H-bridge inverters," IET Power Electron., vol. 3, no. 6, pp. 843–857, Nov. 2010
- [18]. L. Maharjan, T. Yamagishi, H. Akagi, and J. Asakura, "Fault-tolerant operation of a battery-energy-storage system based on a multilevel cascade PWM converter with star configuration," IEEE Trans. Power Electron., vol. 25, no. 9, pp. 2386–2396, Sep. 2010.
- [19]. V. Naumanen, J. Luukko, P. Silventoinen, J. Pyrhonen, H. Saren, and K. Rauma, "Compensation of DC link voltage variation of a multilevel series-connected H-bridge inverter," IET Power Electron., vol. 3, no. 5, pp. 793–803, Sep. 2010.
- [20]. J. Rodriguez, P. W. Hammond, J. Pontt, R. Musalem, P. Lezana, and M. J. Escobar, "Operation of a medium-voltage drive under faulty conditions," IEEE Trans. Ind. Electron., vol. 52, no. 4, pp. 1080–1085, Aug. 2005.