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Analysis of Asymmetrical Cascaded Multi-Cell Multilevel Inverter

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Abstract: Multilevel converters are a very interesting alternative for medium and high power drives. Of these topologies the Multicell group is popularly growing due to its advantages such as modularity and scalability. This paper proposes a new topology of cascaded H bridge Multicell 15 level Inverter which is the mixed form of flying capacitor and cascaded group. This inverter is based on the cascaded connection of cells with reduced no of switches. Multicarrier based level shifting pulse width modulation identified as the most promising technique. This paper presents the most relevant control and modulation method of level shifting pulse width modulation LSPWM for multicell inverters to reduce total harmonic distortion –THD. Simulation results obtained in Matlab/Simulink confirms the effectiveness of the cascaded H bridge multicell 15 level inverter with minimum THD.

Keywords: Cascaded Multicell Inverters. , Multicarrier level shifting pulse width modulation, Total Harmonic Distortion –THD.

I. Introduction

In many applications include Adjustable Speed Drives (ASD), Uninterruptable Power Supplies (UPS),active filters, Flexible AC Transmission System (FACTS),voltage compensators, photovoltaic generators etc., the DC to AC Converters produces an AC output waveform from a DC source. Generally the converters are off two types called as voltage source converters and current source converters. In Voltage Source Inverter (VSIs) have the independent control of output voltage i.e output voltage waveform. Similarly the current source inverter has an independent control of output current. i.e output current waveform. In order to maintain the power quality, the invertrs (convertion of DC to AC by means of power electronic switches) are essential to produce the output voltahe waveform to be followed or to be resembled as that of the sinuaoidal waveform. This can be achieved only by using Multilevel inverters of multiple output levels resembling the sinusoidal shape.

In [1], introduces a bypassed diode technique to the conventional H-bridge multilevel inverter topology which reduces the number of controlled switches used in the system. In [2], introduces H-bridge inverter topology with reduced switch count technique. This technique reduces the number of controlled switches used in conventional multilevel inverter. It dramatically reduces the complexity of control circuit, cost, lower order harmonics and thus effectively reduces total harmonic distortion.

In [3], a new topology for both symmetrical and asymmetrical inverter was suggested. In [4], they have increased the no of output levels so as to improve the quality of a multilevel inverter. It uses an asymmetrically voltage sources with minimum switches than that of the conventional one. In [5],The objective is to make easy, cheap and good multilevel inverter with less number of switches and it explains the working and simulation of a 21-level with the proposed converter topology using less number of switches by PWM technique. In [6], proposes a asymmetrical voltage source multilevel inverter for high voltage and high power applications also it concentrates on reduction of THD.

In [7], It represents a new configuration of three-phase multilevel asymmetrical cascaded voltage source inverter. This structure consists of series-connected sub-multilevel inverters blocks. In [9], a different configuration based on different DC bus voltage for a cascade H-Bridge multilevel inverter. The main objective of this paper is to compare two different symmetrical and asymmetrical arrangements. In [10], a novel three phase multilevel inverter with a small number of switching devices. Multilevel power converter structure has been introduced as an alternative for high power and medium voltage situations.

In this paper the proposed cascaded H bridge multicell multilevel inverter can produce output of 15 numbers of voltage levels with reduced number of switches where the cells are connected in cascaded manner which uses MC-LS-PWM technique to ppproduce the switching signals for the inverter. Also the effectiveness of the inverter is tested with different loads.

II. Multicell Converters

One DC source and two semiconductor switches formed as one cell. Two semiconductor switches connected back to back with DC source. The circuit which is connected with many number of cells is called as Multicell converter.

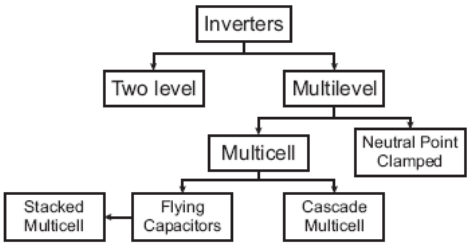

Fig.2.1 Classification of inverters

There are two types of cells in the circuit one is P-cell which produces positive levels and another one is N-cell which produces negative levels. The combinations of these cells are called as Multilevel Multicell inverters.

2.1. Cascaded Multicell Converter (CM).

The Cascaded Multicell converter was introduced by Hammond . This topology is based in the series connection of a three-level output voltage cells, as shown in Fig. 2.2

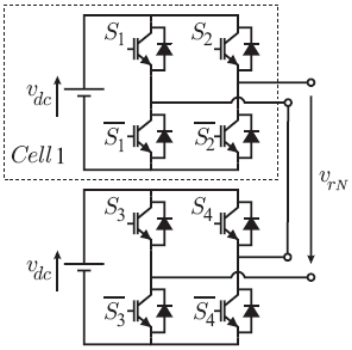

Fig.2.2 4 level Cascaded H bridge Multicell inverters

Each cell is a structure based on an isolated voltage source, so a complex multi-secondary input transformer is required. As the cells are connected in series, the total output voltage corresponds to the addition of the output voltage of each cell

$$\mathrm{VrN} = \sum_{i=0}^{n} \mathrm{Vri} \qquad (1)$$

obtaining a maximum of $2n + 1$ output voltage levels, where n is the number of cells in series per phase. An additional advantage of this topology is that when an internal fault is detected and the faulty cell is identified [10], it can be easily isolated through an external switch, and replaced by a new operative cell, without turn off the inverter [8].

However, while the replacement is done, the maximum output voltage in the faulty leg is reduced to:

$$\hat{v}_f = \hat{v}_{rN}\left(1 - \frac{f}{n}\right) \qquad (2)$$

where f is the number of faulty cells.

2.2. Flying Capacitors (FC).

The Flying Capacitor topology was introduced by Meynard in 1992. This topology is based in the connection of two level cells, as shown in Fig. 2.3, for this reason the maximum number of levels at the output of this converter is:

$$l = n + 1 \qquad (3)$$

,where n is the number of cells connected.

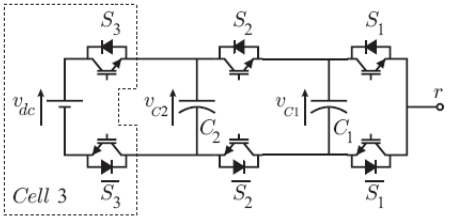

Fig. 2.3. 4-level Flying Capacitor Converter.

For a proper operation, the dc-link voltage on each cell must accomplish with:

$$V_{ci} = I \; V_{dc} \qquad (4)$$

Fortunately, this condition is reached by the inverter itself if the modulation strategy applies the redundancy states in alternate way. Main advantage of *FC* over *CM* converter are that *FC* does not require a complex input transformer and that in case of internal fault of one cell, the number of levels decrease in

$$l_f = l - f \qquad (5)$$

but the maximum output voltage remains constant .

An alternative topology proposed in this paper is mixed multicell converter which has two switches along with a DC source is connected in a cascaded fashion to obtain multivelel outputs. This structure uses a three cells array to produce 15 voltage levels at the output of each leg, as seen in Fig. 2.4.

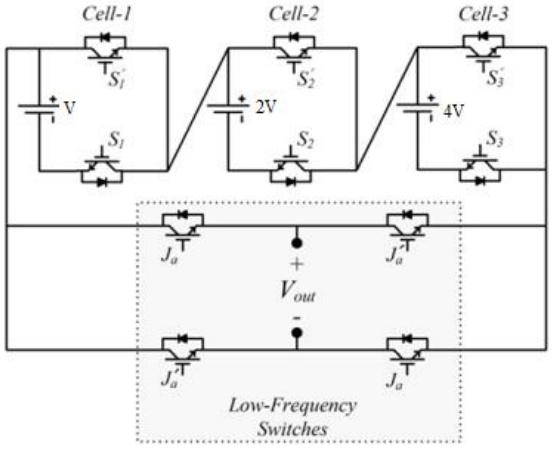

Fig.2.4 Proposed 15 level Cascaded H bridge Multicell inverter.

The main advantages of this approach is that the number of combinations to obtain a desired voltage level is increased . Although it requires less number of capacitors and semiconductors than the other two topologies for the same number of output levels.

III. Control Strategies

3.1 Classification of Control Strategies

Generally the purpose of modulation techniques is to produce the shape of the output waveform as close as to shape of the sinusoidal waveform in order to achieve high efficiency by eliminating the lower order harmonics and there by reducing the total harmonic distortion. Researches on reduction of THD have given rise to many control techniques.

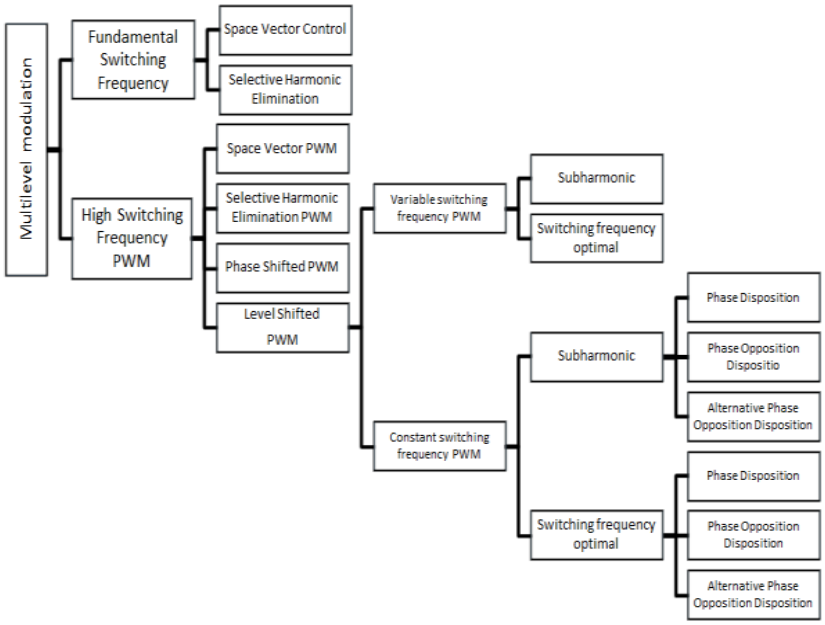

Fig 3.1 Classification of modulation techniques

The fig 3.1 shows the classification of modulation techniques based on their switching frequency of the multilevel inverters. For high switching application the switches (power semiconducters) should have many number of commutations in one fundamental frequency which in turn makes the commutation complex for high switching frequency. Researches on these topics reveals that classic carrier-based sinusoidal PWM (SPWM) with level shifting technique can reduce switching losses and the commutation is made simple.

3.2.1 Multi Carrier Based Level Shifting Pwm (MC-LS-PWM):

Multilevel Inverters requires multiple carriers to produce multiple output voltage levels. In general, m level inverter requires (m-1) carriers. Level shifting means all the carriers have same frequency and also their peak to peak amplitude is also same. The only difference is that there is a level shift between two carrier waveforms.

There are three major kinds of LSPWMs depending on how the carriers are disposed:

- Phase Disposition (PD), where all the carriers are in phase with each other. figure 3.2
- Phase Opposition Disposition Square (POD), where all the carriers above the reference level are in phase among them, but in opposition with those of the below. figure 3.3
- Alternative Phase Opposition Disposition (APOD), where each carrier band is in opposition with each other. figure 3.4

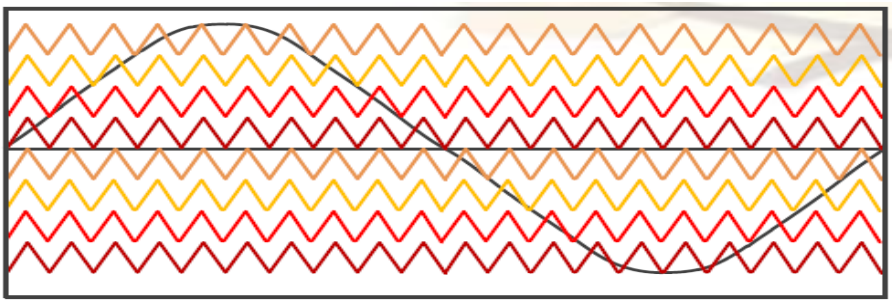

Fig 3.2 Phase Disposition (PD) Level Shifting PWM technique

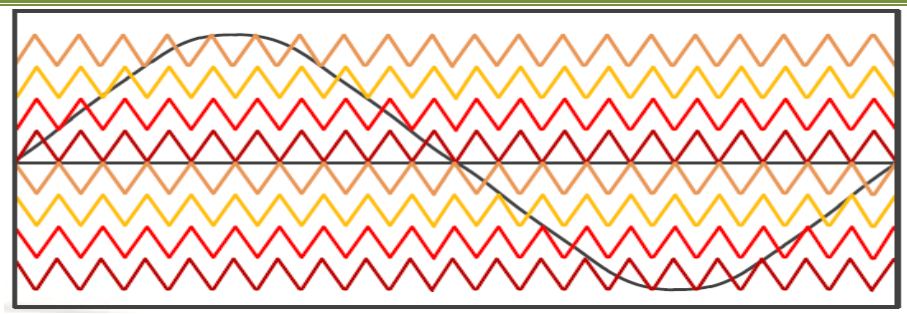

Fig 3.3 Phase Opposition Disposition (POD) Level Shifting PWM technique

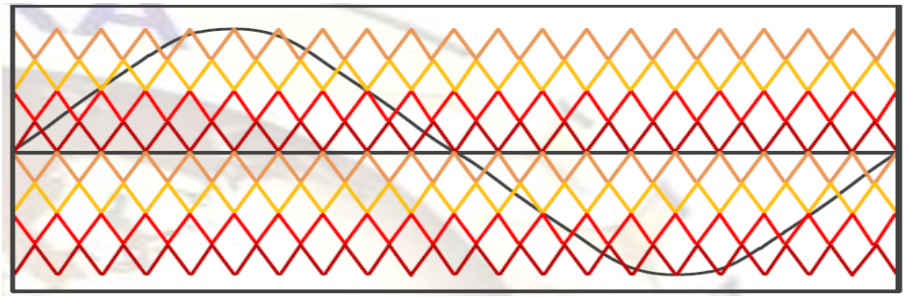

Fig 3.4 Alternate Phase Opposition Disposition (APOD) Level Shifting PWM technique

In this paper we have used the phase disposition (PD) Level Shifting PWM technique. Here we use 14 carriers to produce output of 15 voltage levels. In PD Level Shifting PWM technique all the 14 carriers are having same peak to peak amplitude and their frequencu also same. They differ by their level shifts. In PD all the carriers have same phase disposition. They donot vary with phase. The carrier waveform is shown in the figure 3.2.

IV. Proposed Multicell Multilevel Inverter

A cascade multilevel inverter consists many number of H-bridge (single-phase full bridge) inverter connected in cascaded fashion.. The proposed cascaded multi cell multilevel inverter is a mixed version of cascaded and flying capacitor multi cell inverter. Here the positive switch and the negative switch were connected to the dc source which we call as cell. These cells are connected in cascaded fashion to produce the output levels. Then these voltages are fed through normal single phase inverter o produce the positive and negative voltage levels. The circuit is shown below.

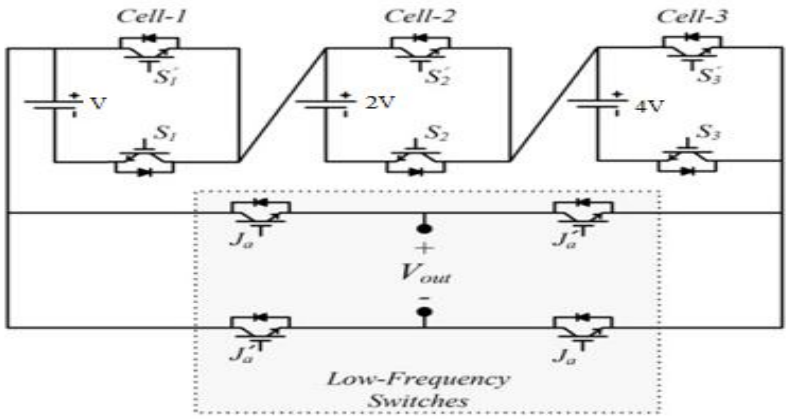

Fig 4.1 Proposed Cascaded H bridge multi cell MLI

In the proposed 15 level inverter we have three cells connected in cascaded fashion. The cell 1 has two switches s1 and s1'. The switch s1 is called positive switch used to produce positive voltage and the switch s1' is called negative switch used to produce negative voltage.

Here we use asymmetric dc voltages whose voltage levels are given as V for cell 1, 2V for cell 2, 4V for cell 3 etc. Each H-bridge has separate dc source. Each SDC (separate D.C. source) is associated with one single-phase full-bridge inverter. The output voltages of each cells are connected in series in order to produce multilevel output at the inverters

Their peak to peak voltage available is the addition of all the voltage sources. In our case the peak to peak voltage is 7V. Here we used voltage V of about 40v. So we produce the output voltage of about 280volts.

The operation is similar to that of the cascaded h ridge inverter. Each cell produces output levels of +V , -V and 0volts.

A fifteen -level cascaded converter, for example, consists of three DC sources and three full bridge converters. The switching pattern to produce 15 voltage levels is shown in the table 4.1

Output voltage levels	Auxillary switches		Main switches					
	Ja	Ja’	S1	S2	S3	S1’	S2’	S3’
7V	1	0	1	1	1	0	0	0
6V	1	0	1	1	0	0	0	1
5V	1	0	1	0	1	0	1	0
4V	1	0	1	0	0	0	1	1
3V	1	0	0	1	1	1	0	0
2V	1	0	0	1	0	1	0	1
1V	1	0	0	0	1	1	1	0
0	0	0	0	0	0	0	0	0
-1V	0	1	1	1	0	0	0	1
-2V	0	1	1	0	1	0	1	0
-3V	0	1	1	0	0	0	1	1
-4V	0	1	0	1	1	1	0	0
-5V	0	1	0	1	0	1	0	1
-6V	0	1	0	0	1	1	1	0
-7V	0	1	0	0	0	1	1	1

Table 3.1 Switching table for15-level asymmetrical Cascade multicell converter.

s.no	components	Cascaded inverter (for one phase)	Proposed multicell inverter (for one phase)
1	Dc sources	7	3
2	Switches	28	10

Table 3.2 Comparison of components between conventional and proposed inverter

V. Simulation Results

5.1 Asymmetrical Cascaded Multicell 15-Level Inverter With Normal Pwm Method with RL load.

5.1.1 Simulation model of single phase asymmetrical cascaded multicell 15-level inverter:

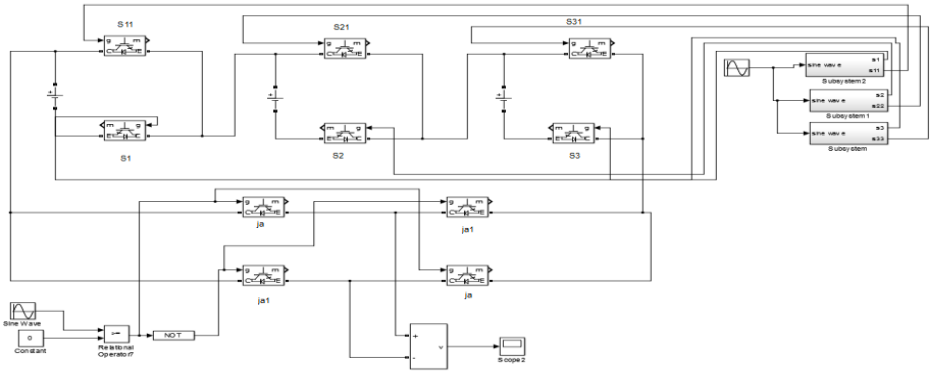

Fig 5.1.1 Simulation model of single phase asymmetrical cascaded multicell 15-level inverter:

5.1.2 Three phase 15 level output voltage waveform employing pulse generator:

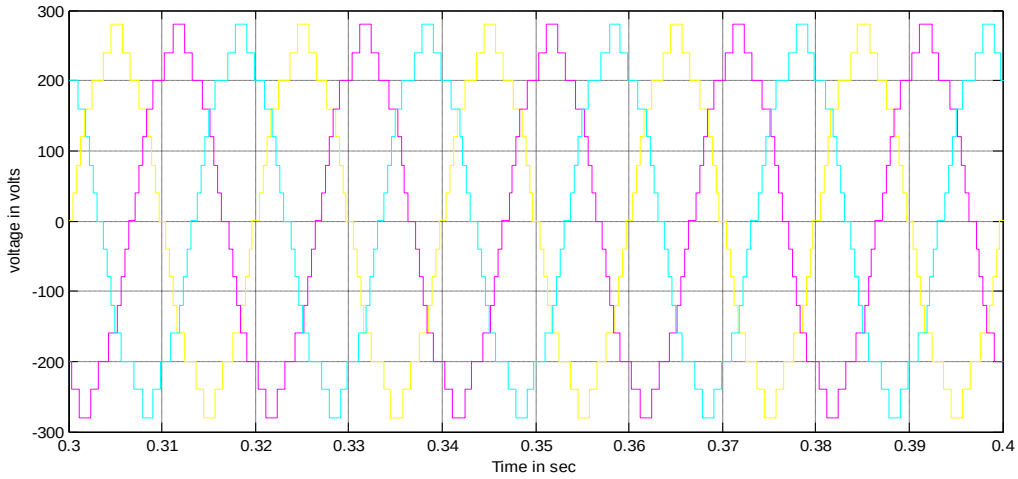

Fig 5.1.2 Three Phase 15 level Output Voltage Waveform employing Pulse Generator:

Fig 5.1.2 Output voltage waveform of 3-phase 15 level Proposed Cascaded H bridge multi cell inverter using pulse generator

The cascaded 15-level inverter output signal is shown in the figure 5.3. The output voltage of 280 volts is produced by using inputs of about 40v, 80v, 160v respectively.

5.1.3 FFT Analysis Using Pulse Generator:

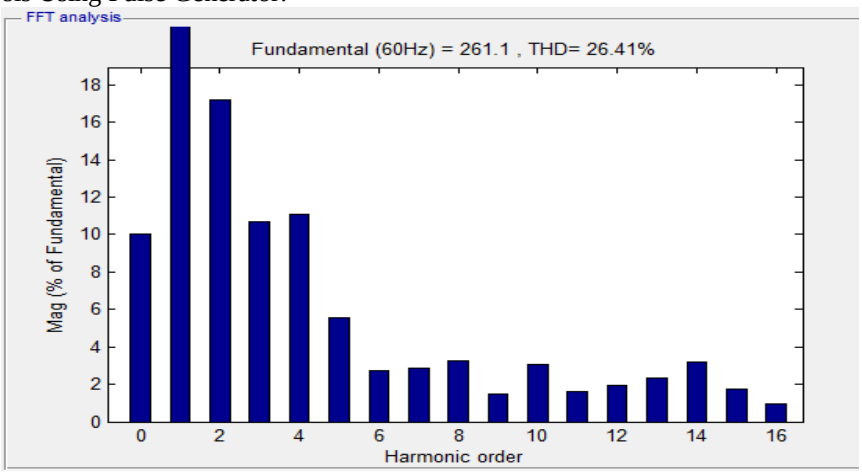

Fig 5.1.3 FFT analysis using pulse generator.

5.2 Simulation with Multi-Carrier Level Shiftng Pwm(MC-LS-PWM):

5.2.1 Waveform Of Multi-Carrier Level Shiftng Pwm (MC-LS-PWM) for 15 levels:

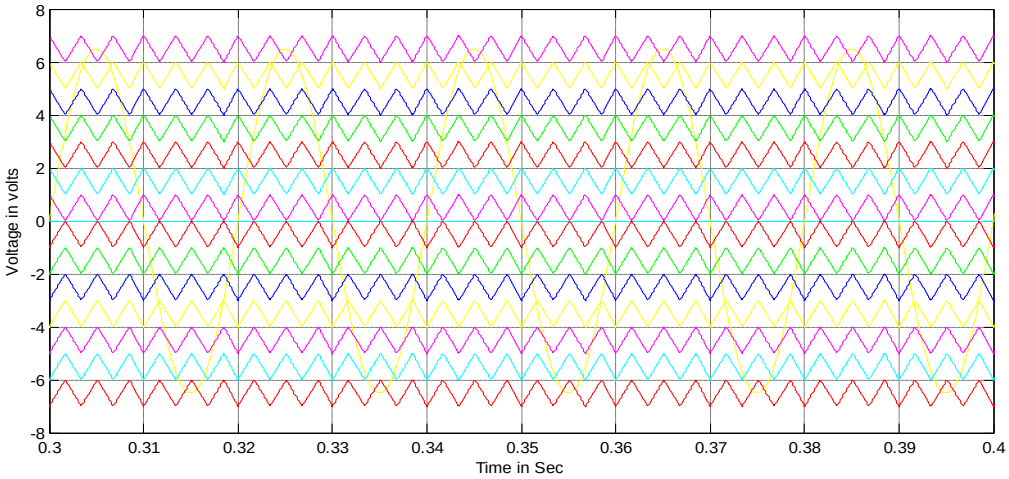

Fig 5.2.1 Waveform Of Multi-Carrier Level Shiftng Pwm (MC-LS-PWM) for 15 levels

5.2.2 Three Phase Voltage Output Waveform using Multi-Carrier Level Shiftng Pwm (MC-LS-PWM) with RL Load

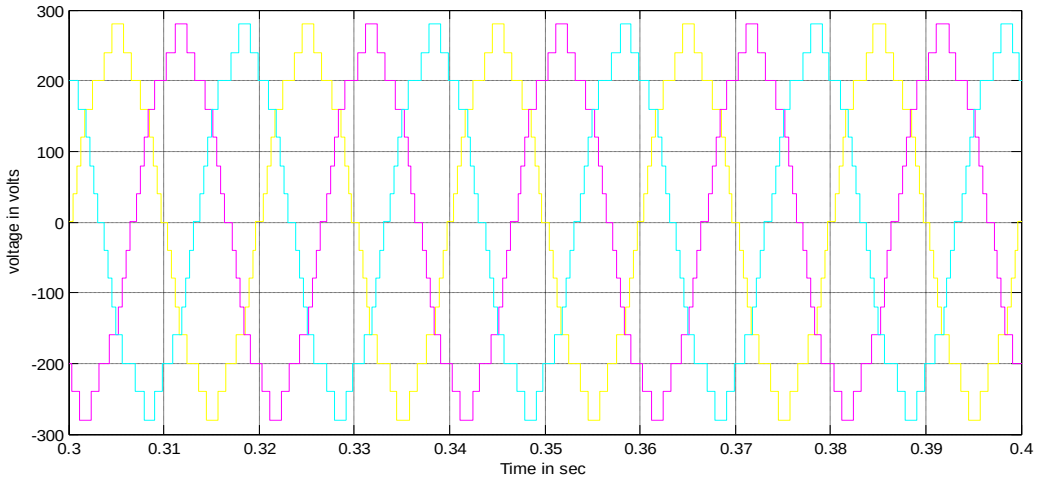

Fig5.2.2 Three Phase Voltage Output Waveform using Multi-Carrier Level Shiftng Pwm (MC-LS-PWM) with RL Load

5.2.3 FFT Analysis Using Multi-Carrier Level Shiftng Pwm (MC-LS-PWM):

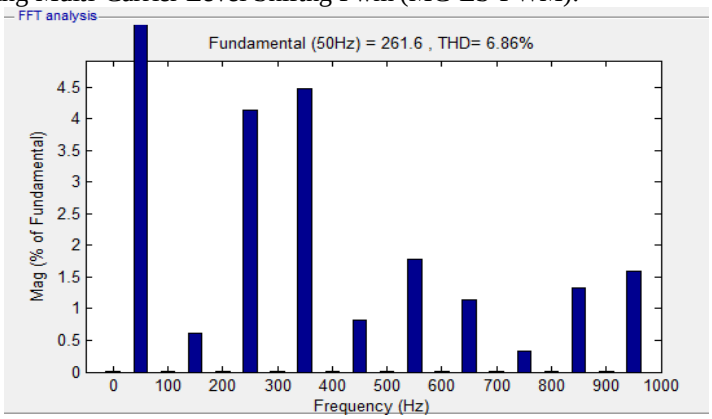

Fig 5.2.3 FFT Analysis Using Multi-Carrier Level Shiftng Pwm (MC-LS-PWM

5.3 Three Phase 15 Level Cascaded Multilevel Inverter Using Level Shifting Multicarrier Pwm (MC-LS-PWM) With Induction Motor Load:

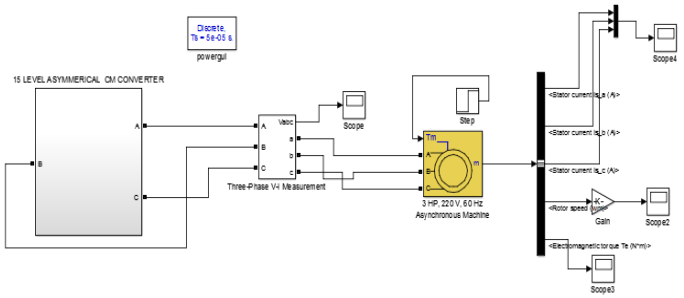

Fig 5.3 Three Phase 15 Level Cascaded Multilevel Inverter Using Level Shifting Multicarrier Pwm (MC-LS-PWM) With Induction Motor Load:

5.3.1 Three Phase 15 Level output voltage Using Level Shifting Multicarrier Pwm (MC-LS-PWM) With Induction Motor Load:

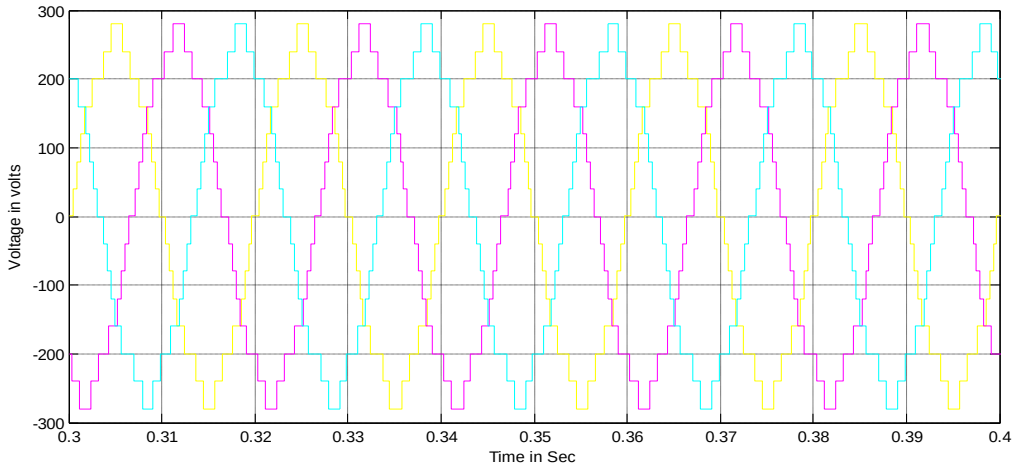

Fig 5.3.1 Three Phase 15 Level output voltage Using Level Shifting Multicarrier Pwm (MC-LS-PWM) With Induction Motor

5.3.2 Three Phase 15 Level output current Using Level Shifting Multicarrier Pwm (MC-LS-PWM) With Induction Motor Load:

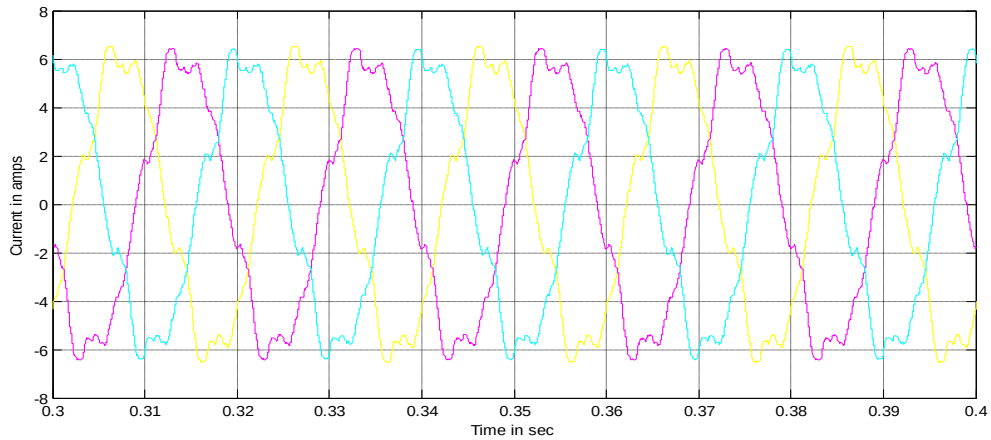

Fig 5.3.2 Three Phase 15 Level output current Using Level Shifting Multicarrier Pwm (MC-LS-PWM) With Induction Motor

5.3.3 Speed Waveform:

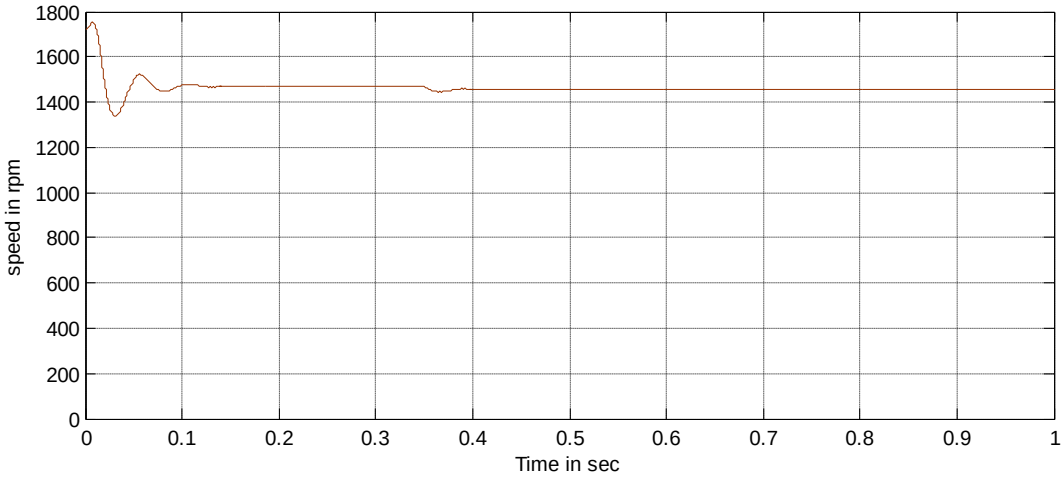

Fig 5.3.3 Speed of the motor with load variations

5.3.4 Torque Waveform:

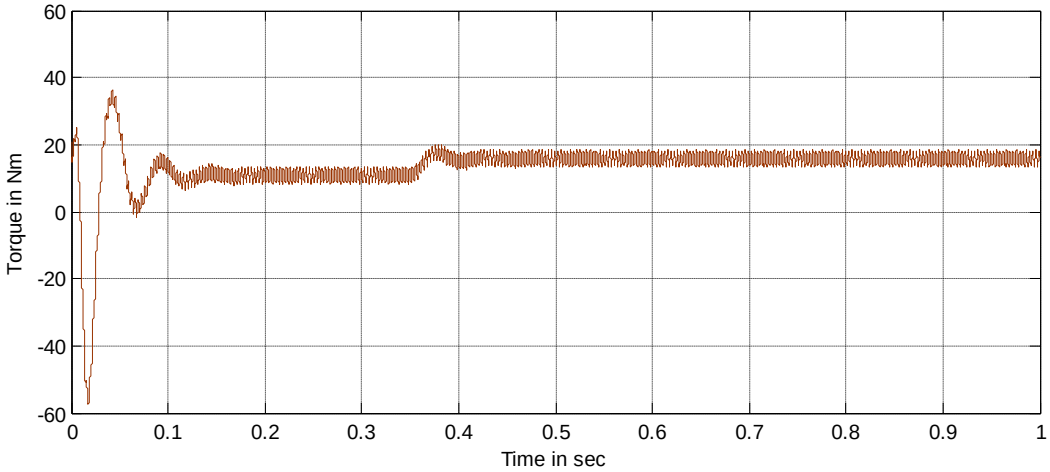

Fig 5.3.4 Torque of the motor with load variations

Conclusion:

The 15 level cascaded multicell inverter was simulated in MATLA simulink. The simulation results shows that the multilevel is achieved with less number of switches with minimum THD. By implementing the LSPWM technique the THD has been further reduced. Since the number of switches has reduced the switching losses reduces and the controller is simple to design and there is no complex calculations in MC-LS-PWM.

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