Integration of RTPG and Activity Driven fine grained CG using Stack approach

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Abstract: In Integrated circuits a gargantuan portion of chip power is expended by clocking system which comprises of timing elements such as flipflops, latches and clock distribution network. This paper enumerates power efficient design of shift registers using D flipflops along with Clock and Power gating integration. Clock gating and power gating proves to be very effective solutions for reducing dynamic and active leakage power respectively. The two techniques are coupled in such a way that the clock gating information is used to drive the control signal of power-gating circuitry. In this paper, an activity driven fine-grained clock and power gating is proposed. First, a technique named Optimized Bus-Specific- Clock-Gating (OBSC) is introduced which reduces the problem of gated flipflop selection by appropriate selection of subset of flipflops. Then another technique named Run Time Power Gating (RTPG) is proposed for power gating the combinational logics performing redundant operations. The proposed shift registers are designed up to the layout level with 1V Power supply in 0.18um technology and simulated using microwind simulations for different clock frequencies and the performance of the shift registers are evaluated by observing the average power.

Keywords: Optimized Bus-Specific-Clock- Gating (OBSC), Run Time Power Gating (RTPG), microwind..

Introduction:

With the smaller geometries in Deep Sub-Micron (DSM) technology, the number of gates that need to be integrated on a single chip, power density, and total power are increasing rapidly. Also, designing for low- power has become increasingly important in a wide variety of applications. However, creating optimal low-power designs involves trade such as timing versus power and area versus power at the di_erent stages of the design ow. Successful power-sensitive designs require engineers to have the ability to accurately and e_ciently perform these trade.

To address these issues directly, it is essential to understand the di_erent types and sources of power dissipation in digital Complementary Metal Oxide Semiconductor (CMOS) circuits. The reason for choosing the CMOS technology is that it is currently the most dominant digital IC implementation technology. Power dissipation in CMOS digital circuits is categorized into two types: peak power and time-averaged power consumption. Peak power is a reliability issue that determines both the chip lifetime and performance. The voltage drop e_ects, caused by the excessive instantaneous current owing through the resistive power network, a_ects the performance of a design due to the increased gate and interconnect delay. This large power consumption causes the device to overheat which reduces the reliability and lifetime of the circuit. Also noise margins are reduced, increasing the chance of chip failure due to crosstal structure, since the clock gating logic will sit in the clock tree.

CMOS digital circuits occurs in two forms: dynamic and static. Dynamic power dissipation occurs in the l ogic gates that are in the process of switching from one state to another. During this process, any internal and external capacitance associated with the gate's transistors has to be charged, thereby consuming power. Static power dissipation is associated with inactive logic gates (i.e., not currently switching from one state to another). Dynamic power is important during normal operation, especially at high operating frequencies, whereas static power is more important during standby, especially for battery-powered devices

For dynamic loss reduction we are using Clock Gating technique and for static loss reduction we are suing RTPG technique explained below.

Clock Gating and Power Gating

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states. Switching states consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred.[1]

Clock gating works by taking the enable conditions attached to registers, and uses them to gate the clocks. Therefore it is imperative that a design must contain these enable conditions in order to use and benefit from clock gating. This clock gating process can also save significant die area as well as power, since it removes large numbers of muxesand replaces them with clock gating logic. This clock gating logic is generally in the form of "Integrated clock gating" (ICG) cells. However, note that the clock gating logic will change the clock tree

Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. In addition to reducing stand-by or leakage power, power gating has the benefit of enabling Iddq testing.

Integrated Clock and Power Gating

Clock Gating and Power Gating are two most commonly used design methods to save dynamic and leakage power respectively. How about integrating the two solutions such that they complement each other? In this post, I will talk about a simple way to do so.

Clock Gating is accomplished by using Clock Gating Integrated Cell *(CGIC)* which gates the clock to the sequential elements present in its fan-out when the enable signal is logic 0. Power Gating structures may be of two types: Simple Power Gating and State Retention Power Gating. Using the former technique, the output of the logic gates slowly leaks the charge at the output and thereby when the *SLEEP* signal is de- asserted, one cannot predict the logic value at the output. The latter technique is able to retain the state at the output which was last present before asserting the *SLEEP*signal.

Let's take up a few plausible scenarios:
- Case I - Normal Case: Which employs only conventional clock gating. It is depicted in the figure.

Clock Gating Integrated Cell
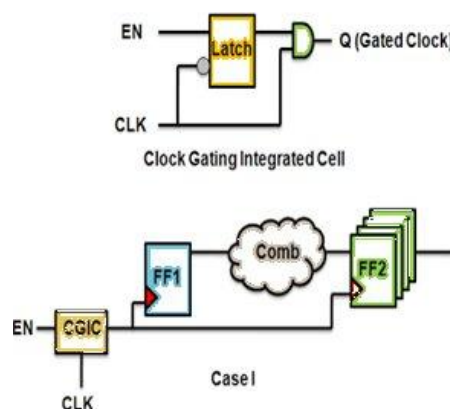
Case I

- Case II - When one does not need to retain the states of the combinatorial cells or the sequential elements. One possible scenario could be in the case of a standalone IP, which is not comunicating with any other IP on the SoC. Here one can use thee simple power gating where the SLEEP signal is derived from the CGIC itself using a latch, as depicted in the figure below. Doing so, we would save both dynamic and leakage powers.

Modified Clock Gating Integrated Cell
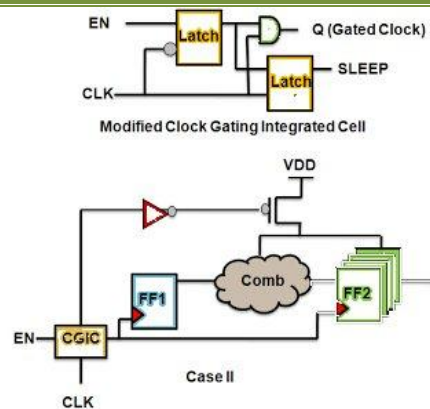
Case II

- Case IIII - When one does not need to retain the states of the combinatorial cells, but the sequential outputs need to be safe-stated. Possible use-case could be where only the sequential outputs communicate with other IPs on the SoC. This can be accomplished by using State Retention Flip Flops instead of the conventional flip-flops.
- Case IV - When both the combinatorial cells and the sequential cells interact with other IPs. But the previous value need not be required. Since it is a classic case of interaction between "switchable power domain" with" always ON", it entails the use of isolation cells between such power domain crossings. It must be noted that in such a case, isolation cell would always be present in the always ON power domain, i.e., it would receive it's VDD supply from the always ON power domain supply. This is because, when the switchable power domain in OFF, the isolation cell can function only if receives the power supply!
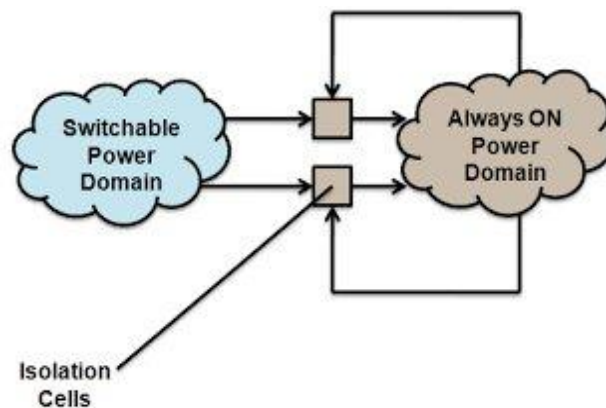
Isolation Cells

Isolation Cells can be simple cells like AND or an OR gate, which receive one input in a way that, irrespective of the second input coming from the switchable power domain, the value would be controllable. For example, logic 0 for AND gate and logic 1 for an OR gate. I will try to take this up in a separate post.
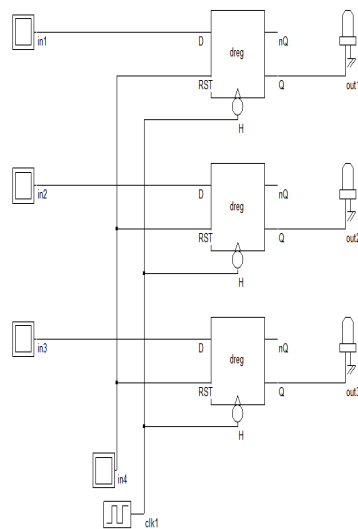
Here we classified the shift register to three places

Fig: Non Clock Gating Circuit.

PROPOSED OBSC

Optimized Bus Specific Clock Gating is very effective technique to maximize dynamic power reduction as shown in fig.3. It chooses only a subset of flip-flops (FF) to be gated selectively, and the problem of gated FF selection is reduced from exponential complexity into linear. It works by comparing the inputs and outputs and gates the clock when they are equal [11]. Considering N FFs in the non-CG circuit, each FF can be chosen as gated or nongated. Hence, 2N CG solutions are possible and the exponential complexity problem is reduced into linear. Assume that all the FFs are chosen to be gated initially, then the problem is in determining which FFs should be excluded from gating [1]. Heuristically, the FF with the maximum output data toggle rate should be excluded from gating first. This is because that maximum output data toggle rate indicates that minimum clock toggles will be gated, thus power will reduce least or even increase if the FF is gated. More formally, the FF with the maximum output toggle rate is excluded from gating first, then the FF with the second largest output toggle rate is excluded and so on until all the FFs are excluded (i.e., the original non CG circuit). Apparently, during the process of exclusion, there will be N+1 possible CG solutions which is linear complexity.
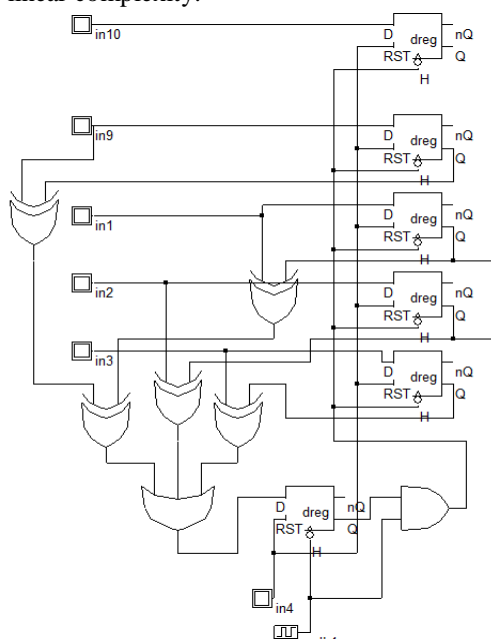

Fig: PBSC circuit

In order to achieve integration of CG and RTPG, apply OBSC technique to the design, then a subset of FFs is clock gated. During the clock gated period, the outputs of the gated FFs are stable. Consequently, those combinational logics whose inputs only depend on gated FF outputs will be inactive and can be power gated as shown in Fig 6.(a). For each output of the power gated cell, whether a connection to primary output presence has to be checked. A holder logic should be added in order to avoid signal floating. Suppose that four out of five FFs are clock gated. The circled cells are completely dependent on the stable gated FF outputs, so they are not active and can be power gated into sleep [1]. However, one input of the XOR gate i is the output of ungated FF A, and one input of the AND gate h is the primary input. Since both the ungated FF output and PI may not be stable during the clock gated period, the XOR gate i and the AND h may be active. So they should not be power gated. In order to avoid floating signal, a holder should be placed at the output of each power gated cell if that output connects to non power gated cells or primary outputs (Pos)

If RTPG has to be applied, a footer (high- Vth CMOS transistor) between the actual ground and virtual ground of the power gated cells should be added. After the integration of CG and RTPG, the low power design should look like Fig.6 (b).The enable signal generated from OBSC is used as the sleep signal for the PG. The cells that are totally dependent on gated FF outputs are power gated. Holders are placed between the power gated cells and the non power gated cells so that the non power gated cells can function properly
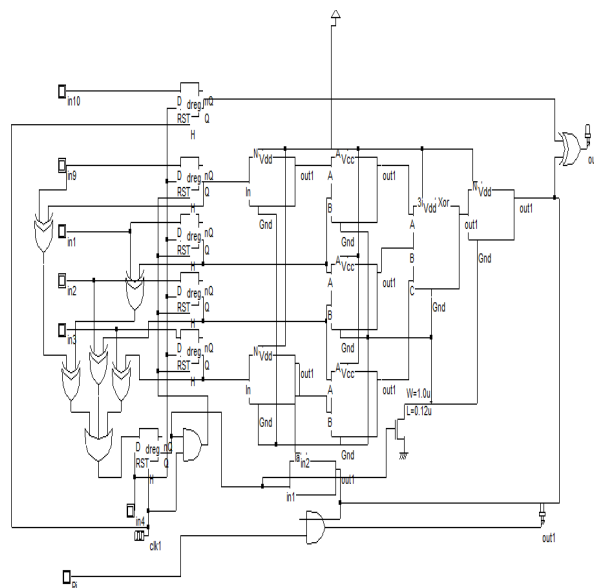

Fig: Integration of OBSC and RTPG

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Stack approach:

This is another new leakage reduction technique, which we call the stack approach
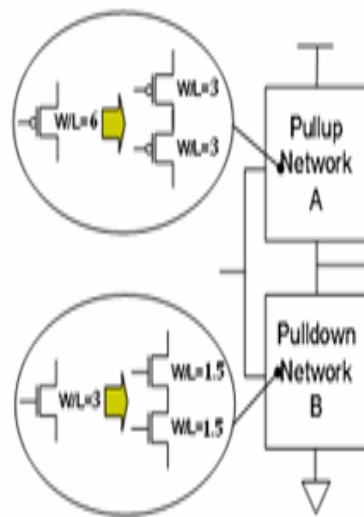
Fig: Structure of variable body biasing technique with sleep method

Another technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half size transistors.   When the two transistors are turned off together, induced reverse bias between the two transistors results in sub-threshold leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach. It divides the w/l ratio into two equal parts.
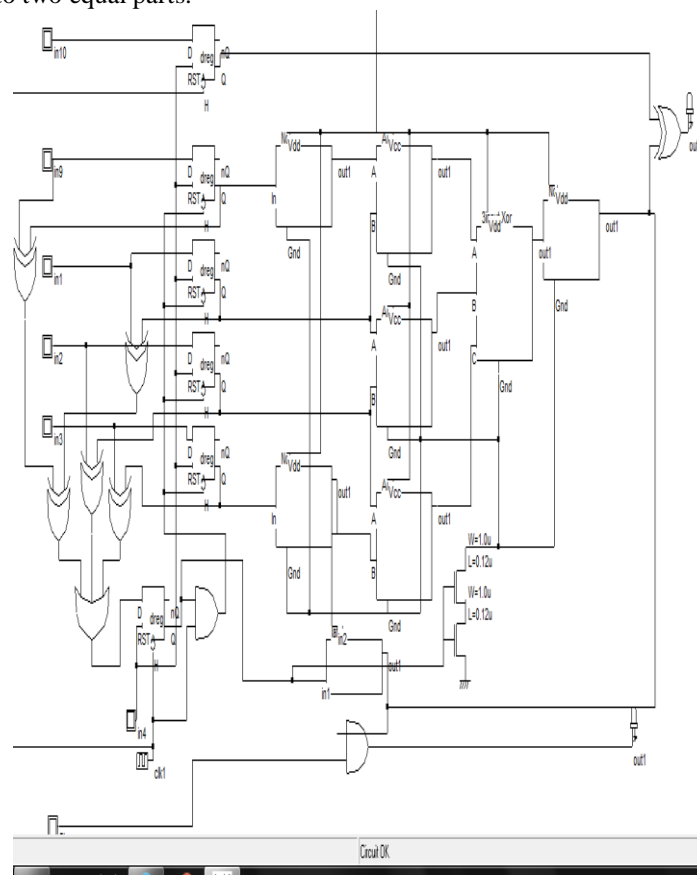

Fig: Integration of OBSC and RTPG with Stack approach

Tabulation

Circuit	Power Dissipaion
Integration of OBSC and RTPG with sleep	0.305mW
Integration of OBSC and RTPG with Stack approach	0.163mW

Conclusion:

In this Paper, a fine-grained CG and RTPG integration is achieved in sequential circuits. First, an activity driven fine-grained OBSC technique is evaluated that selects only a subset of FFs to gate . Moreover, the clock enable signal generated in the OBSC circuit can be used as the sleep signal in RTPG. Following this, Sequential circuits that implements both OBSC and RTPG is considered and their performances are evaluated with sleep and stack technique.

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