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Design of Nano-Electro Mechanical (NEM) Relay Based Nano Transistor for Power Efficient VLSI Circuits

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Abstract: In this paper, the Nano-electro mechanical (NEM) relay is experimentally demonstrated and the proposed NEM relay based transistor is used to implement the digital circuit for the efficient power utilization. Nano-electro mechanical is one of the promising technologies for the Complementary Metal-oxide Semiconductor CMOS backend design. The reductions of the power utilization are advancement of the Integrated Circuit (IC) technology. The NEM relay based transistor is designed by using the bulk CMOS technology then the transistor is used to implement the digital circuits. In this work, the NEM relay based inverter is designed in the Tanner EDA by using CMOS technology. The proposed NEM based digital inverter is performed efficiently compare than the conventional CMOS based digital inverter. The synthesis of the conventional and proposed work is evaluated with the spice net list file by using the H-Spice. By implementing the NEM Relay based digital inverter, the power utilization is highly reduced compare than the bulk CMOS technology and also the area utilization is efficient. The NEM Relay Nano transistor based inverter is implemented in terms of the VLSI Design environment.

Keywords: Nano-electro mechanical (NEM), Complementary Metal-oxide Semiconductor (CMOS), Integrated Circuit (IC), Very large scale integration (VLSI).

Introduction

In the early 21st century, the Nanotechnology is one of the promising impacts for the semiconductor industry. Nanotechnology is basically known as the technology, which can perform on the Nano scale area. In nanotechnology, the biological systems of the real world applications and productions are ranging from the separate molecules to submicron dimensions. The elaboration of the integrated circuit (IC) measured by the multiple number of transistors integrated into single chip. This leads to increase the transistor counts as well as power. Voltage source (Vdd) of the transistors is not proportionally reduced with the size of transistors; therefore, the increase of the transistors counts as well as the density. To achieve the efficient system performance, either the digital circuits essential to perform with the slow speed or the circuits operate periodically disconnected from the voltage source. These conditions are increasing the OFF-state current (I_{OFF}).

In MOSFET circuits, the transistors are basically constructed to allow the input voltage source and to perform at a specified output voltage. Conventional CMOS technology scaling has significantly improve the performance of the digital circuits but it also leads to the cost. The threshold voltage scaling is further improving the power consumption. Sustained scaling of the voltage source is degrading the performance of the parallel circuit.

Various parameters are changed to achieving the largest level of integration and also the numbers of transistor counts have reduced to fabricate the multiple functions on a single chip. However, the power utilization, voltage has minimized along with increased frequency ranges. FinFET conducting a channel protected by a thin silicon 'fin'. FinFET technology providing the efficient leakage current compare with CMOS technology, but the Memory capacity is also increased. Hence, the leakage current is one of the challenging technologies for the Memory designers. Nano-electro-mechanical (NEM) relay devices provide an attractive solution with the switching characteristics and perform with the high sub-threshold slope than the CMOS devices. NEM relay devices have near ideal I-V characteristics, affect from a minimum mechanical delay compared to the electrical delay of CMOS Circuit. For circuit design applications, the NEM relay technology is still relatively trend with devices established with the area in the 10's of Microns. However, the NEM relay achieves the energy-delay characteristics better than the CMOS over a high range of frequencies. In this research work, the Verilog-A model for novel NEM relay transistor is implemented by using nm technology. NEM relay transistor based logical circuits is implemented with the efficient power utilizations compare than the CMOS based logical circuits.

Related Works

These NEM switches are performing with the efficient advantageous over than the CMOS devices. Generally, CMOS technology perform with minimum energy limit per operation due to the OFF-state leakage current (I_{OFF}). Tsu-Jae King Liu et al., 2010 presented the advanced improvements in electrostatic Nano-relay design methodologies. Scaling of the MOSFET devices is mainly used to improve the energy efficiency. Nano-relays are necessity to perform with the low ON-state resistance (R_{ON}). Compare to CMOS transistors, the NEM-relay devices has zero OFF-state leakage current and minimum voltage range. Alexis Peschot et al., 2015 described the energy efficiency of the NEM-relay switches.

OFF-state leakage current (I_{ON}) of the transistors controlled the energy efficiency of the CMOS devices. In case of mechanical switches, the entire devices operate with the zero off state leakage current. Basically, the IC design is limited by the tradeoff between the power, delay and area. Body biasing is one of the effective mechanisms to adjust the tradeoff between the power and computational delay. Hei Kam et al., 2009 explained the Nano relay technology for achieving the high reliability. Nano-electro-mechanical (NEM) relay switches have better advantages than the CMOS devices due to the ideal supply voltage source (V_{DD}).

The reduction of the supply voltage (V_{DD}) is minimizing the dimensions of the relay into the sub micron. Hei Kam et al., 2011 presented the scaling characteristics of the NEM-relays for ultra low power digital logic. The sub-threshold swing of the MOSFET transistors is one of the main issues in the CMOS devices. Nano-electro- mechanical (NEM) switches have been proposed to perform with the efficient power utilizations due to the zero off state current. The same MOSFET dimensional scaling is applied to the NEM relay is further improving the device density. Fixed capacitance value is used to increase the actuation area and also the increasing level of voltage source is further reducing the energy.

Chuang Qian et al., 2017 stated the computations of the electro mechanical relays to achieve the zero off state current. Reduction of the hysteresis voltage is one of the main challenges of the electro-mechanical relay due to the constant minimum voltage source. Implementations of the ICs with CMOS transistors perform with the lower energy efficiency due to the imperfection of the electronic devices. Basically, the NMOS devices used as the pull down network and PMOS devices used as the pull up network in CMOS circuits. A mechanical logical relay performs to both pull up and pull down network depend on the body bias voltage. Md Torikul Island Badal et al., 2016 explained the CMOS design of current comparator based 130nm technology.

The current comparator is used for the current steering (CS) applications in the digital to analog conversion (DAC). Wilson current mirror circuit is used as the input stage in the DAC. The amount of current is flowing from one form of device into another form of device is achieved by the current mirror circuit. Ankur Goel et al., 2014 described the design of SRAM based power gating technique in nano CMOS technology. Improving the amount of supply voltage through the standby mode diode transistor is used to reduce the leakage current. Power gating technique is used to reduce the leakage current of the CMOS device. Compare with the CMOS technology, the FinFET devices are offer the efficient power consumptions. By using reverse bias of the device is one of the method is used to reduce the sub-threshold leakage current.

Triple well technology is required to support the reverse bias of the device and the negative supply voltage is required for the reverse bias technique. The negative voltage generation of the device is not possible in the small and medium memory element areas. Power gating technique is also used to reduce the power utilizations. Increasing of the supply voltage is highly achieved by using the ground gating technique. The voltage trimmable power gating technique is offer the efficient power consumptions.

Nano-Electro Mechanical (NEM) Relay Structure and Operation

In NEM-Relay transistor, the movable poly-SiGe gate deferred over a tungsten drain, source and body. When the voltage difference between the gate and body terminals (V_{gb}) is higher than the threshold input voltage (V_{tiv}), the gate dislocates towards the body by the electro static force. The source and drain terminals are summarized due to the actuated state in the conductive channel. When the (V_{gb}) is lower than the threshold output voltage (V_{tov}), the air gap between the drain and source terminals change to the gate original state. In that state, the electrical isolation is occurred between the channels. The relay is turned into the ON stage by the occurrence of the sufficient electro static force in the drain and source.

NEM Relay Circuit Characteristics

In the four terminal relay, there are two possible states like ON and OFF state. When there is reverse voltage source in the gate and body, the short occur between the drain and source terminals. This characteristic is same in the conventional CMOS devices. The body terminal biasing to the Gnd, then the device will be in on state like an NMOS device. Likewise, the device is performing like a PMOS device when body terminal is

biasing to Vdd. However, in CMOS circuits, the body terminal is entirely independent device. That body terminal is not able to bias at reference voltages. This characteristic is providing some advantages of the custom designs and some cases the signals connected to the both gate and body to perform like a X-or gate. The structure of Nano-electro-mechanical (NEM) Relay is shown in Figure.1.

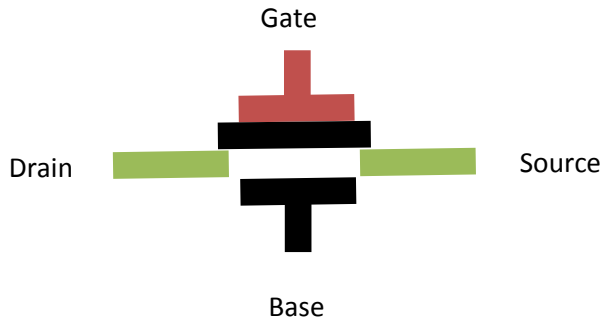

Figure 1: Nano-electro-mechanical (NEM) Relay

Modeling of the NEM Relay Circuit

In NEM Relay circuit, the entire circuit switching delay is suffered by the electrical delay by the mechanical motion of the single relay. The required discharge time of the channel from ON state into a capacitive load is determined by the modeling of the resistance and capacitance of the ON state channel. In the resistance of the tungsten wires, the ON state resistance is one of the parts of the channel (R_{trace}), the channel resistance (R_{ch}), the resistance of the source and drain (R_{con}), endurance of the device is increased by the passivating oxide (R_{pox}). The load capacitance of the device is used to calculate the electrical delay. The internal structure of NEM Relay based nano transistor is is illustrated in Figure 2.There are various parasitic capacitors are available in the load presented device. In between the gate and body air cap, the several capacitors are formed. The gate to channel capacitance is fluctuated due to the relay Off-state so the capacitance is provided in relay On-state.

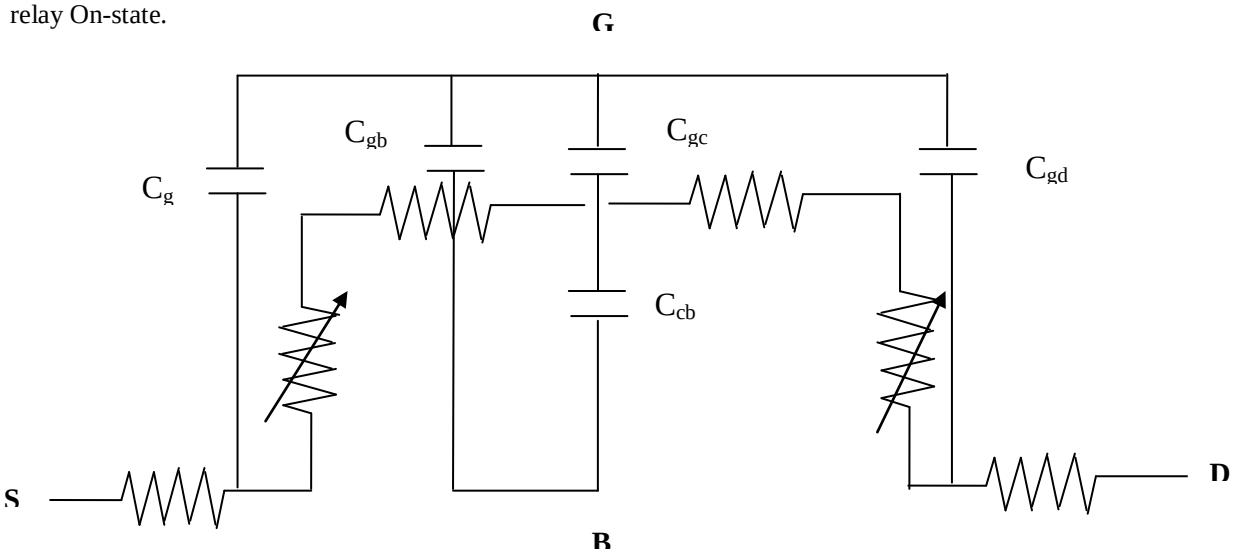

Figure 2: Internal structure of NEM-relay based Nano Transistor

NEM Relay Nano Transistor Based Digital Circuit Design

In this section, the pass gate style NEM based inverter is designed by using nano transistor. The voltage transfer characteristics of the pass gate style NEM Inverter with single input held at 10 v promote the hysteresis for the NEM inverter. The devices are On and Off due to the minimum voltage swing. That voltage source is depending on the device pull-in voltage and the variations of the device to device voltage are occurred due to the deposition process. Compare to CMOS, the NEM relay devices are independent of the drain and source voltages. Nano-inverter design is illustrated in Figure 3

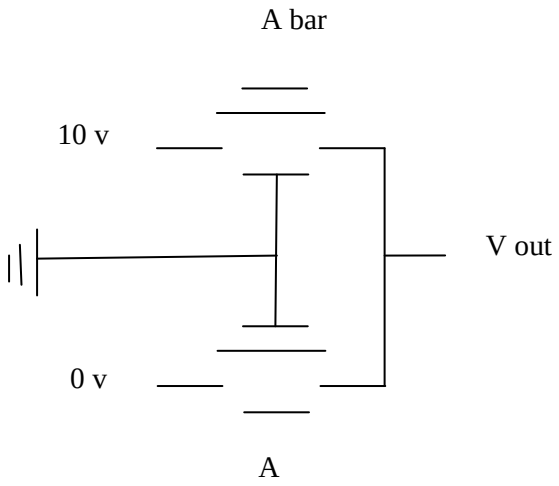

Figure 3: NEM-Relay Nano Transistor based Inverter design

The relay based devices are performed when the device turned into the ON stage with increased level of gate voltage that is it operates similarly like a NMOS transistor. The drain to source current (Ids) varied due to the ON and OFF stages of the devices. When the gate voltage is decreasing, the PMOS transistors are turned to ON stage with the positive body biasing voltage. The CMOS devices are high speed functions and also the NEM devices are low power functions. Hybrid CMOS/NEM technology based digital circuits are perform with the both advantages of the CMOS devices as well as the NEM devices. For example, the CMOS/NEM inverter design is operate with the low power utilizations and the cell stability is improved. To achieve the high manufacturing is one of the main challenges in the NEM relay based logical circuits. These relay devices are incorporated using carbon nano tubes or nano wires. By applying the body bias voltage, the operating voltage source of the device is further decreased.

Mapping From CMOS Into NEM Relay

Inequity between the electrical and mechanical delays recommend, the relay based optimized logical circuits are used to minimize the mechanical delay. Those, reduction are achieved by the alignment of mechanical movement. Mapping from CMOS into NEM Relay is shown in Figure 4. The NEM relay based logic circuits are designed by using the single complex gate. Only the complexity of the NEM devices is the extension of the electrical delay due to the device collapsibility.

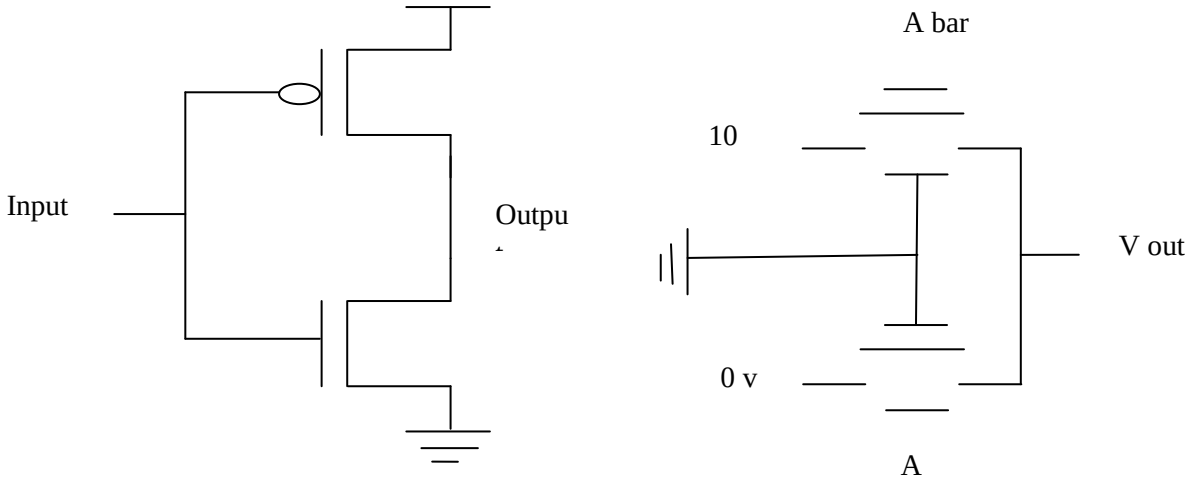

Figure 4: Mapping from CMOS into NEM Relay

Scaling of the NEM Relay Circuit

The NEM-relay based logical circuits are expected to perform with the minimum switching voltages and minimum delay. To achieve the efficiency, the NEM-relay based digital circuit's physical dimensions are scaled. The power utilization per operation is increased by decreasing the load capacitance and also the operating voltage source also decreased. Minimum gap thickness is further decrease the pull in voltage source. To achieve the fast actuation, the scaling process of the device is more quickly than the spring constant. The reduction of the power utilization cannot be further reduced in the performance improved devices. After the disconnection of electrical force, the spring is relocating to the un-actuated position. For the device ON and OFF, the minimum number of power is set to the device. The scaling process will minimize the spring force of the device. Thus, the real energy utilizations of the device are evaluated in the circuitry level.

Results and Discussions

The Nano-electro Mechanical (NEM) Relay Switch based Nano transistor is designed by using CMOS Technology with the efficient Nano technology. The proposed Nano transistor is implemented in the digital circuits like inverters to check the functional characteristics. The Nano-transistor based inverter is performed efficiently in terms of the VLSI Design environment with the minimum number of logical elements utilization and power utilization. These simulation results for proposed design are illustrated in the Fig.5.

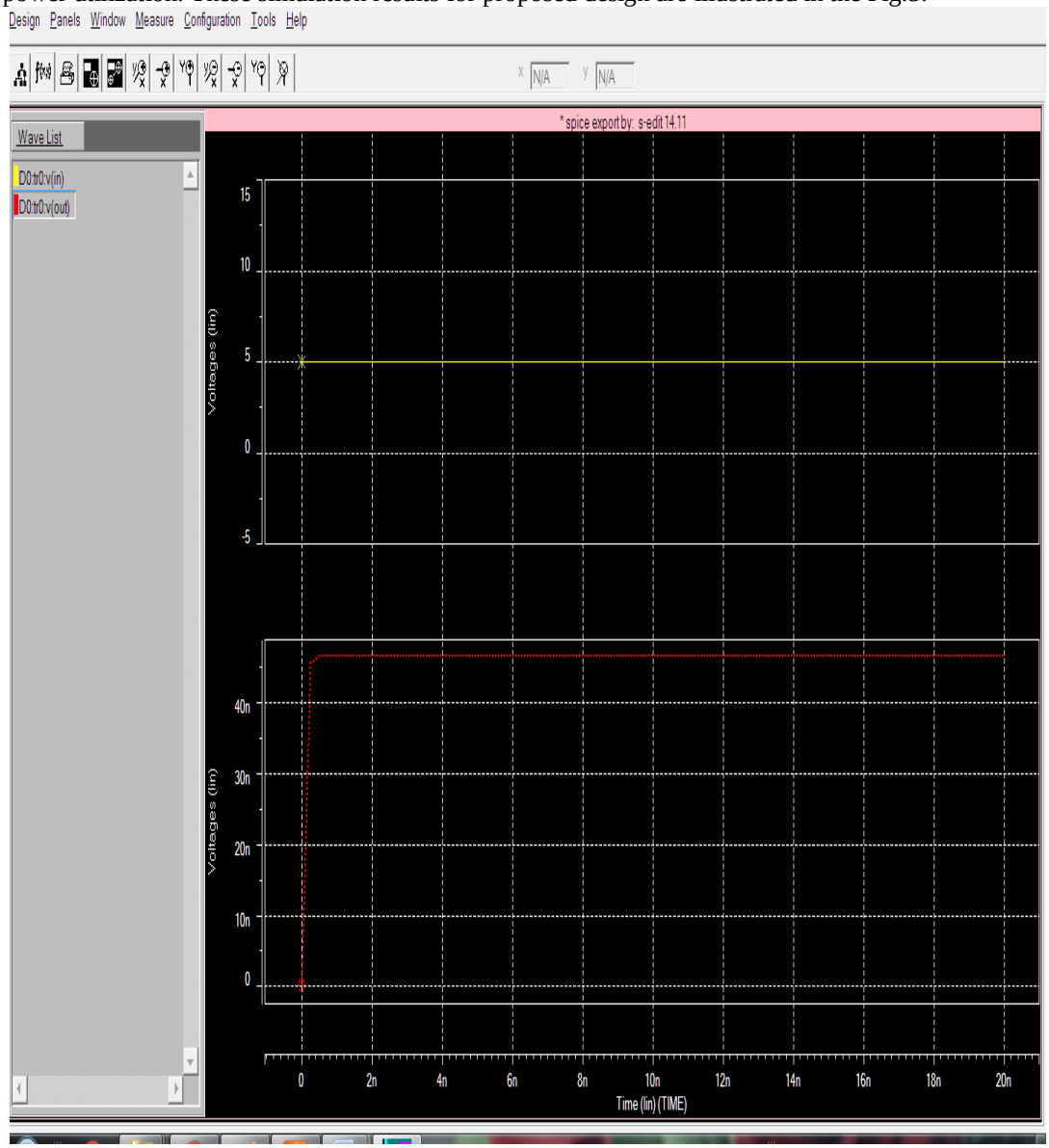

Figure 5: Simulation Result for Proposed NEM Relay based Inverter

Table 1: Tabulation of Synthesis Result for Conventional and Proposed Power Analysis

Description	**Conventional Inverter**	**Proposed NEM relay based Inverter**
Peak-Power	3.8600 E-09	1.000 E-09

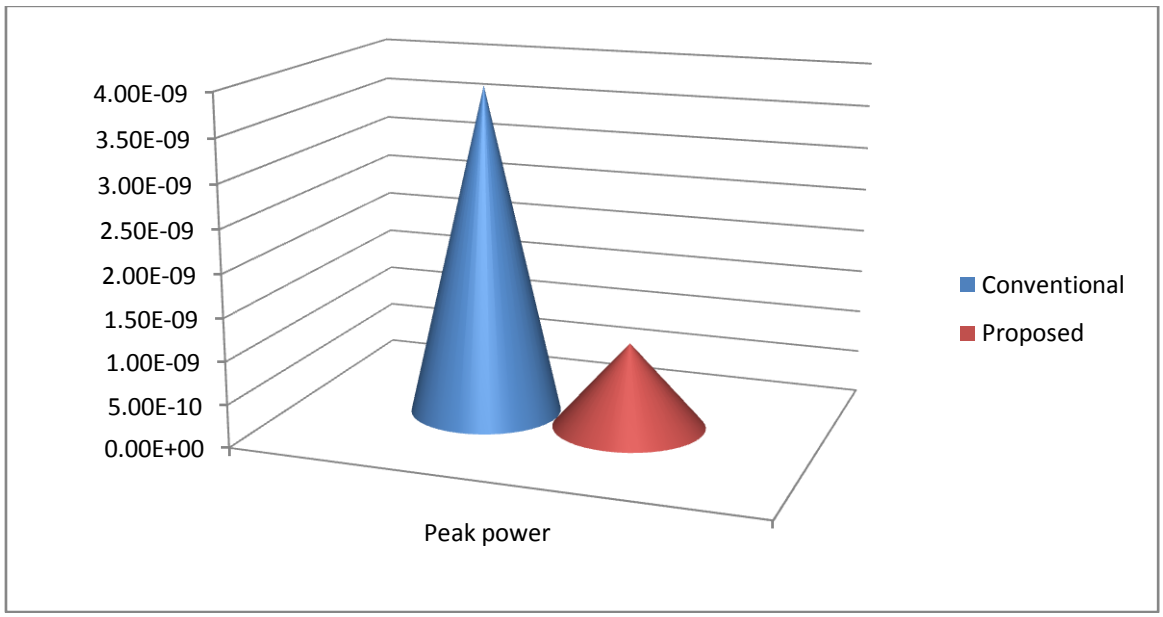

Figure 6: Graphical Representation of Synthesis Result for Conventional and Proposed Power Analysis

Conclusion

The general drawback of the bulk CMOS devices are forced to implement the logic technology to achieve the efficient power efficiency in the semi conductor industry. Nano-electro mechanical (NEM) relay is used to provide the efficient power consumptions compare than the general CMOS technologies. NEM Relay is one of the promising technologies for power utilization. These NEM relay nano transistor based digital circuits are evaluated by using H-Spice. Nano transistor based digital circuit is compared with the bulk CMOS based circuit and the performance of the proposed work is evaluated. In future, the power utilizations are achieved by using the Carbon Nano-tube Tunnel FET (CNTFET) based CMOS design.

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